

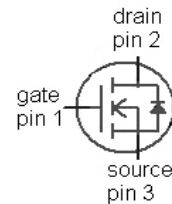
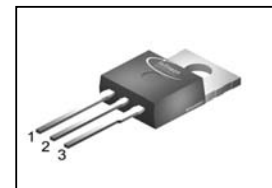
OptiMOS® 2 Power-Transistor
Features

- Ideal for high-frequency dc/dc converters
- Qualified according to JEDEC¹⁾ for target application
- N-channel - Logic level
- Excellent gate charge x $R_{DS(on)}$ product (FOM)
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 175 °C operating temperature
- dv/dt rated
- Pb-free lead plating; RoHS compliant

Product Summary

| | | |
|------------------|------|------------|
| V_{DS} | 30 | V |
| $R_{DS(on),max}$ | 12.8 | m Ω |
| I_D | 30 | A |

PG-TO220-3-1



| Type | Package | Marking |
|--------------|--------------|---------|
| IPP13N03LB G | PG-TO220-3-1 | 13N03LB |

Maximum ratings, at $T_j=25$ °C, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|-------------------------------------|----------------|---|-------------|-------------|
| Continuous drain current | I_D | $T_C=25$ °C ²⁾ | 30 | A |
| | | $T_C=100$ °C | 30 | |
| Pulsed drain current | $I_{D,pulse}$ | $T_C=25$ °C ³⁾ | 120 | |
| Avalanche energy, single pulse | E_{AS} | $I_D=30$ A, $R_{GS}=25$ Ω | 64 | mJ |
| Reverse diode dv/dt | dv/dt | $I_D=30$ A, $V_{DS}=20$ V, $di/dt=200$ A/ μ s, $T_{j,max}=175$ °C | 6 | kV/ μ s |
| Gate source voltage ⁴⁾ | V_{GS} | | ± 20 | V |
| Power dissipation | P_{tot} | $T_C=25$ °C | 52 | W |
| Operating and storage temperature | T_j, T_{stg} | | -55 ... 175 | °C |
| IEC climatic category; DIN IEC 68-1 | | | 55/175/56 | |

¹⁾ J-STD20 and JESD22

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Thermal characteristics

| | | | | | | |
|-------------------------------------|------------|--|---|---|-----|-----|
| Thermal resistance, junction - case | R_{thJC} | | - | - | 2.9 | K/W |
| SMD version, device on PCB | R_{thJA} | minimal footprint | - | - | 62 | |
| | | 6 cm ² cooling area ⁵⁾ | - | - | 40 | |

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

| | | | | | | |
|----------------------------------|---------------|--|-----|------|------|---------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}, I_D=1\text{ mA}$ | 30 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=20\text{ }\mu\text{A}$ | 1.2 | 1.6 | 2 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$ | - | 0.1 | 1 | μA |
| | | $V_{DS}=30\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$ | - | 10 | 100 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$ | - | 1 | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=4.5\text{ V}, I_D=20\text{ A}$ | - | 15.2 | 18.9 | m Ω |
| | | $V_{GS}=10\text{ V}, I_D=30\text{ A}$ | - | 10.7 | 12.8 | |
| Gate resistance | R_G | | - | 1 | - | Ω |
| Transconductance | g_{fs} | $ V_{DS} >2 I_D R_{DS(on)max}, I_D=60\text{ A}$ | | 57 | - | S |

²⁾ Current is limited by bondwire; with an $R_{thJC}=2.9\text{ K/W}$ the chip is able to carry 47 A.

³⁾ See figure 3

⁴⁾ $T_{j,max}=150\text{ °C}$ and duty cycle $D<0.25$ for $V_{GS}<-5\text{ V}$

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

⁵⁾ Diagrams are related to straight lead versions.

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics

| | | | | | | |
|------------------------------|--------------|---|---|------|------|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$ | - | 1019 | 1355 | pF |
| Output capacitance | C_{oss} | | - | 364 | 485 | |
| Reverse transfer capacitance | C_{rss} | | - | 49 | 74 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=15\text{ V}, V_{GS}=10\text{ V},$ $I_D=20\text{ A}, R_G=2.7\ \Omega$ | - | 4 | 7 | ns |
| Rise time | t_r | | - | 4 | 6 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 16 | 24 | |
| Fall time | t_f | | - | 2.8 | 4.2 | |

Gate Charge Characteristics⁶⁾

| | | | | | | |
|------------------------------|---------------|---|---|-----|-----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=15\text{ V}, I_D=40\text{ A},$ $V_{GS}=0\text{ to }5\text{ V}$ | - | 4.0 | 5 | nC |
| Gate charge at threshold | $Q_{g(th)}$ | | - | 1.6 | 2.2 | |
| Gate to drain charge | Q_{gd} | | - | 2.3 | 3.5 | |
| Switching charge | Q_{sw} | | - | 5 | 7 | |
| Gate charge total | Q_g | | - | 8 | 10 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 3.9 | - | |
| Gate charge total, sync. FET | $Q_{g(sync)}$ | $V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }5\text{ V}$ | - | 7 | 9 | nC |
| Output charge | Q_{oss} | $V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$ | - | 8 | 11 | |

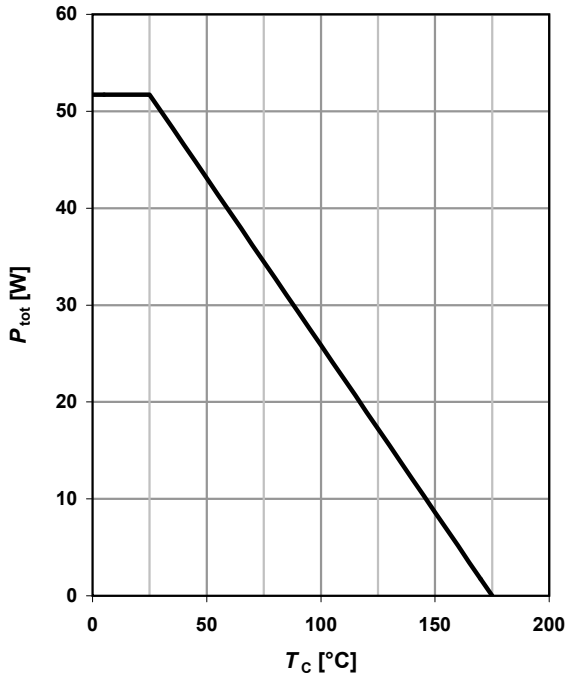
Reverse Diode

| | | | | | | |
|----------------------------------|---------------|---|---|------|-----|----|
| Diode continuous forward current | I_S | $T_C=25\text{ }^\circ\text{C}$ | - | - | 78 | A |
| Diode pulse current | $I_{S,pulse}$ | | - | - | 120 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_F=80\text{ A},$ $T_j=25\text{ }^\circ\text{C}$ | - | 1.23 | 1.2 | V |
| Reverse recovery charge | Q_{rr} | $V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$ | - | - | 10 | nC |

⁶⁾ See figure 16 for gate charge parameter definition

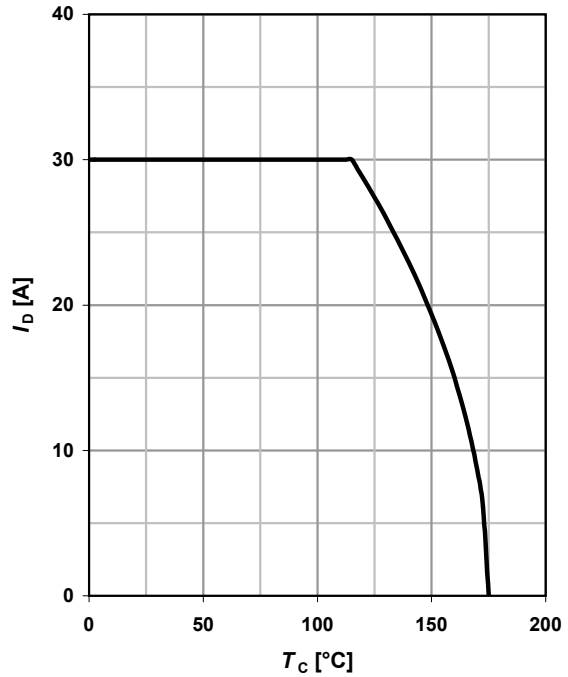
1 Power dissipation

$$P_{tot} = f(T_C)$$



2 Drain current

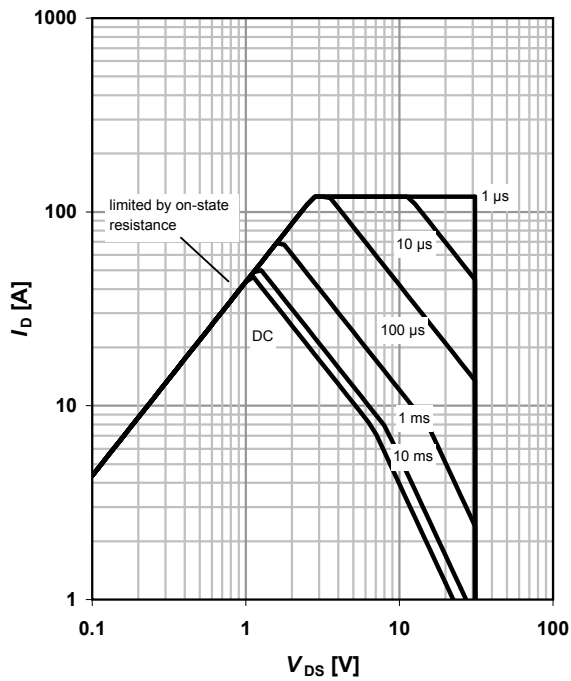
$$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$$

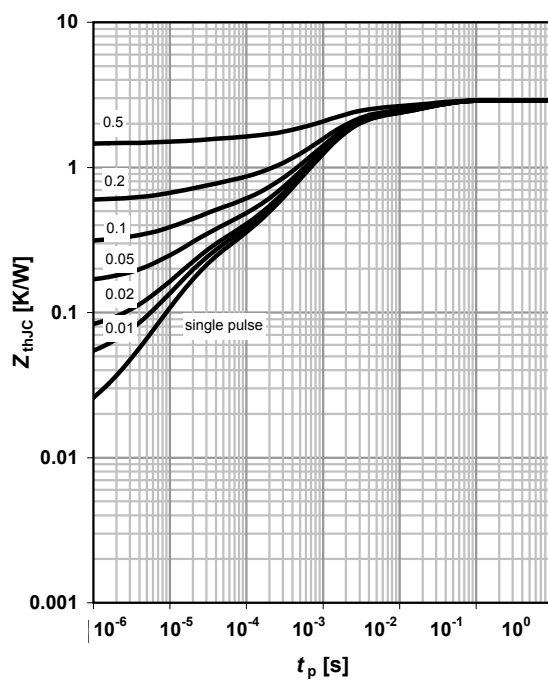
parameter: t_p



4 Max. transient thermal impedance

$$Z_{thJC} = f(t_p)$$

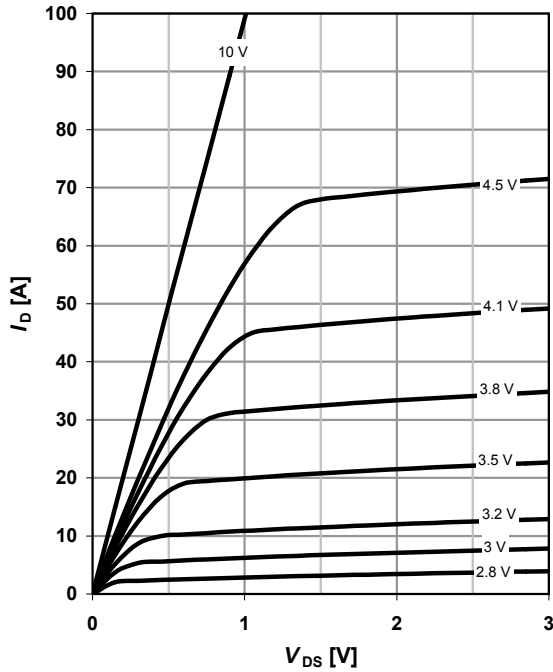
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

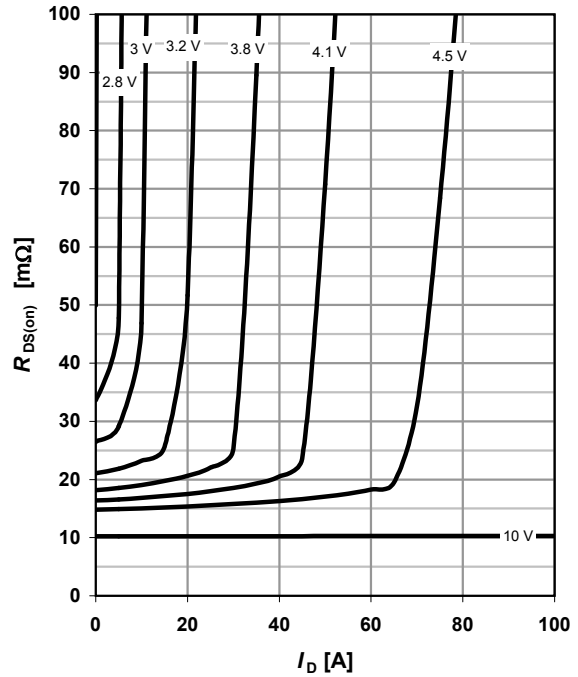
parameter: V_{GS}



6 Typ. drain-source on resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

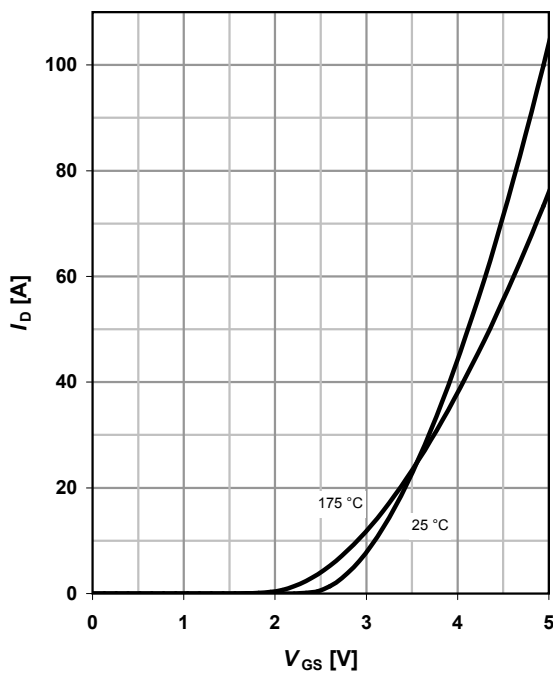
parameter: V_{GS}



7 Typ. transfer characteristics

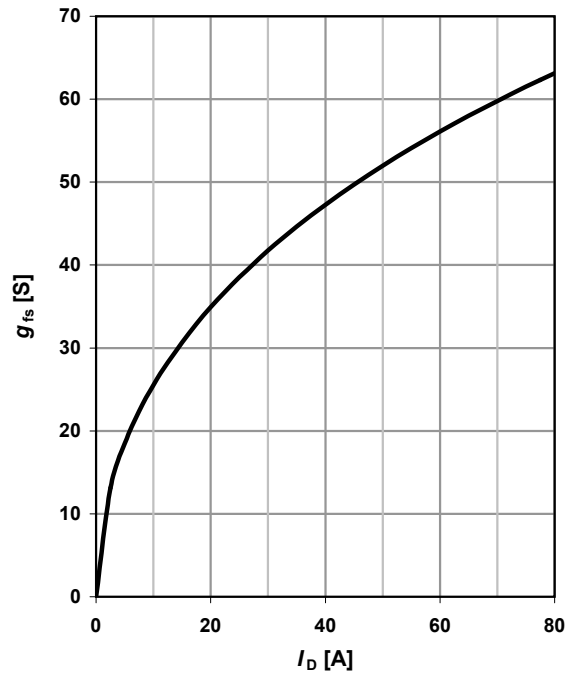
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter: T_j



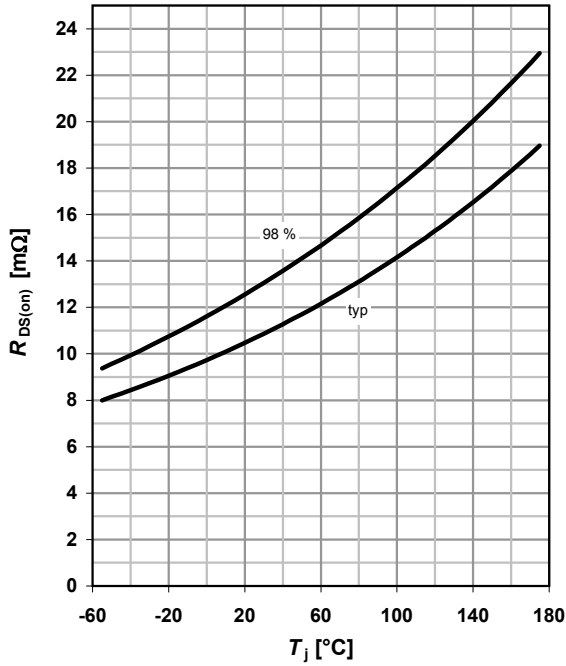
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



9 Drain-source on-state resistance

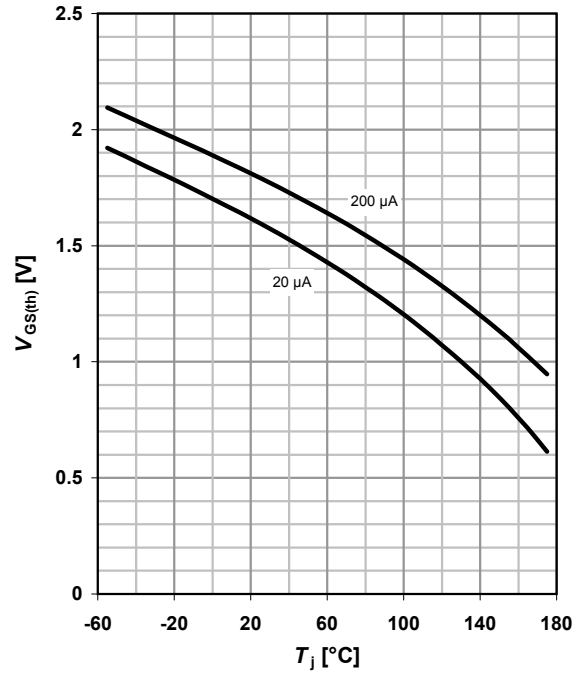
$$R_{DS(on)} = f(T_j); I_D = 50 \text{ A}; V_{GS} = 10 \text{ V}$$



10 Typ. gate threshold voltage

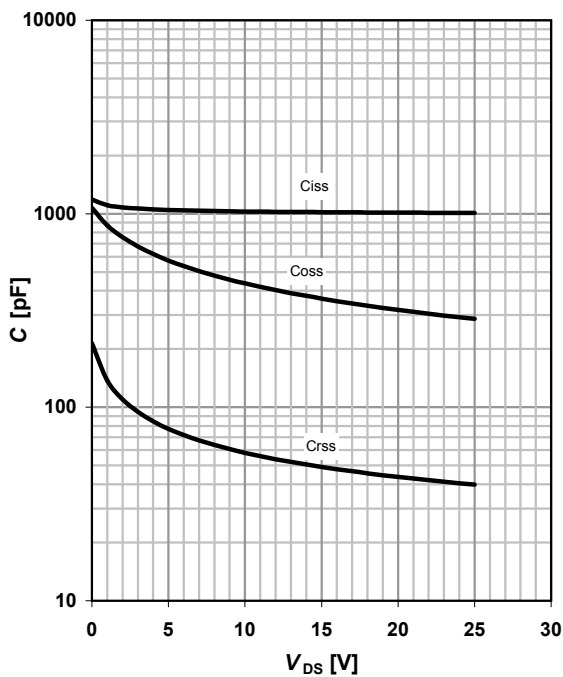
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. Capacitances

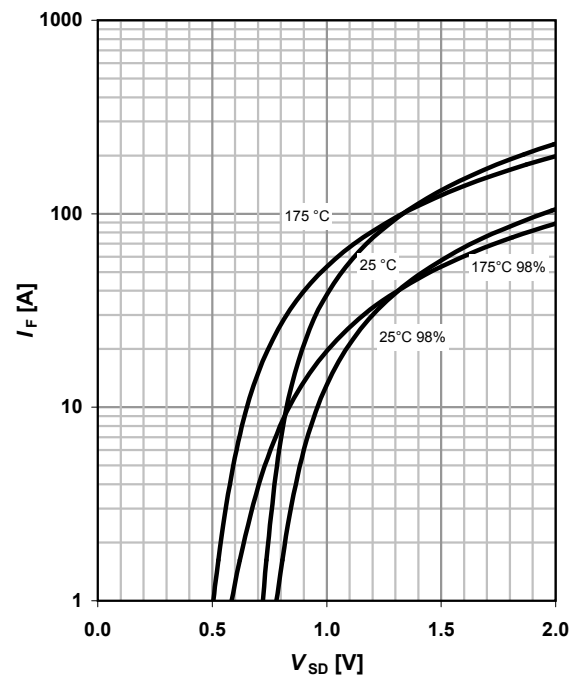
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



12 Forward characteristics of reverse diode

$$I_F = f(V_{SD})$$

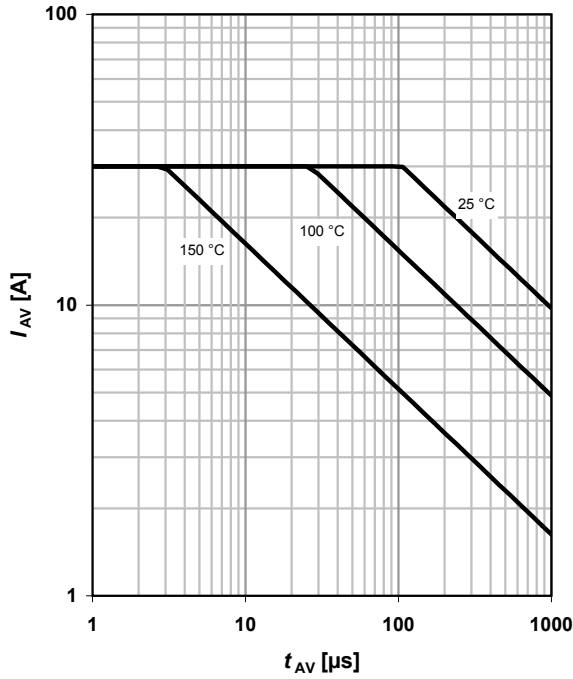
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

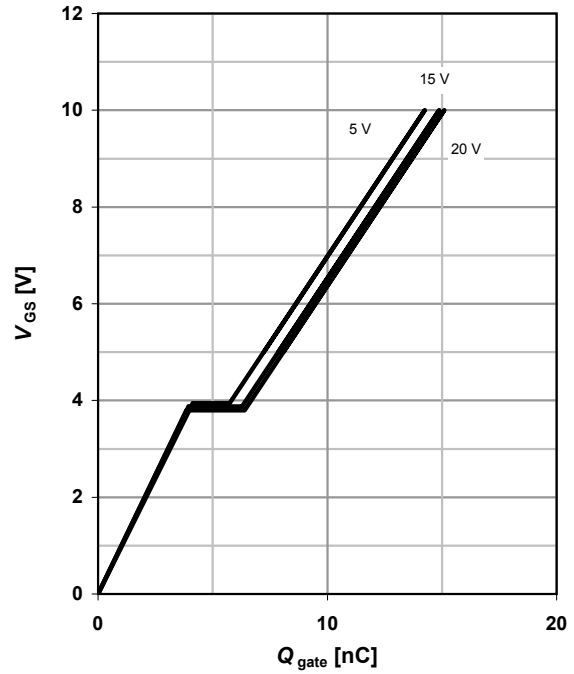
parameter: $T_{j(start)}$



14 Typ. gate charge

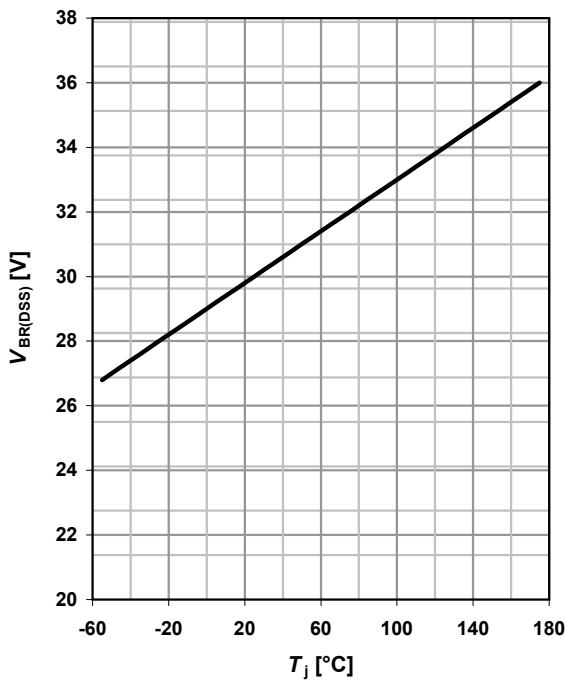
$V_{GS}=f(Q_{gate}); I_D=40 \text{ A pulsed}$

parameter: V_{DD}



15 Drain-source breakdown voltage

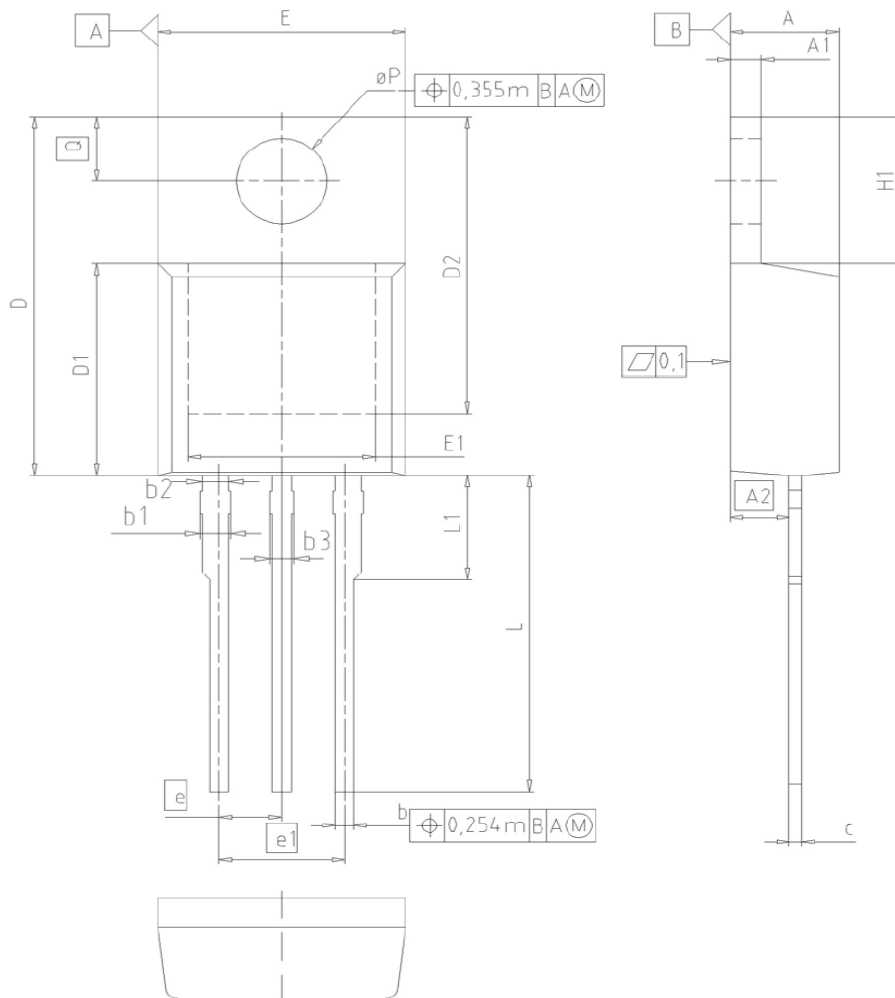
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$



16 Gate charge waveforms



PG-TO220-3-1



| DIM | MILLIMETERS | | INCHES | |
|----------|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.30 | 4.57 | 0.169 | 0.180 |
| A1 | 1.17 | 1.40 | 0.046 | 0.055 |
| A2 | 2.15 | 2.72 | 0.085 | 0.107 |
| b | 0.65 | 0.86 | 0.026 | 0.034 |
| b1 | 0.95 | 1.40 | 0.037 | 0.055 |
| b2 | 0.95 | 1.15 | 0.037 | 0.045 |
| b3 | 0.65 | 1.15 | 0.026 | 0.045 |
| c | 0.33 | 0.60 | 0.013 | 0.024 |
| D | 14.81 | 15.95 | 0.583 | 0.628 |
| D1 | 8.51 | 9.45 | 0.335 | 0.372 |
| D2 | 12.19 | 13.10 | 0.480 | 0.516 |
| E | 9.70 | 10.36 | 0.382 | 0.408 |
| E1 | 6.50 | 8.60 | 0.256 | 0.339 |
| e | 2.54 | | 0.100 | |
| e1 | 5.08 | | 0.200 | |
| N | 3 | | 3 | |
| H1 | 5.90 | 6.90 | 0.232 | 0.272 |
| L | 13.00 | 14.00 | 0.512 | 0.551 |
| L1 | - | 4.80 | - | 0.189 |
| ϕP | 3.60 | 3.89 | 0.142 | 0.153 |
| Q | 2.60 | 3.00 | 0.102 | 0.118 |

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